

High Voltage C-V Measurement System : CS-605A/CS-603A

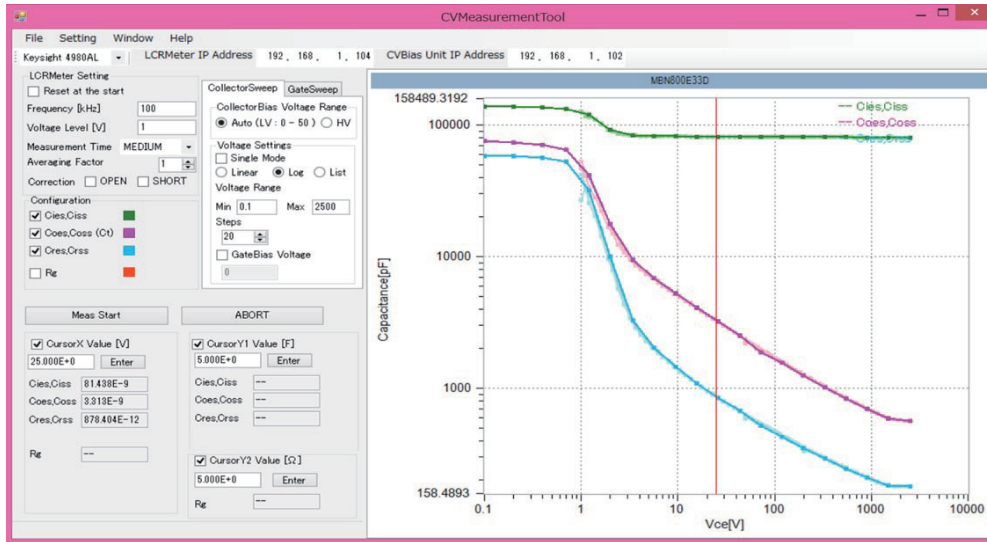
Capacitance measurement of devices for power electronics such as SiC, GaN, High-voltage capacitor & etc.

- Automatic measurement on capacitances at 5kV(CS-605A)/3kV(CS-603A) with sweep
- Test adaptors for curve tracer can be used for various device package types
- System up with probe station for capacitance measurement on Wafer & on Chip
- High and low temperature test in chamber with external interlock function



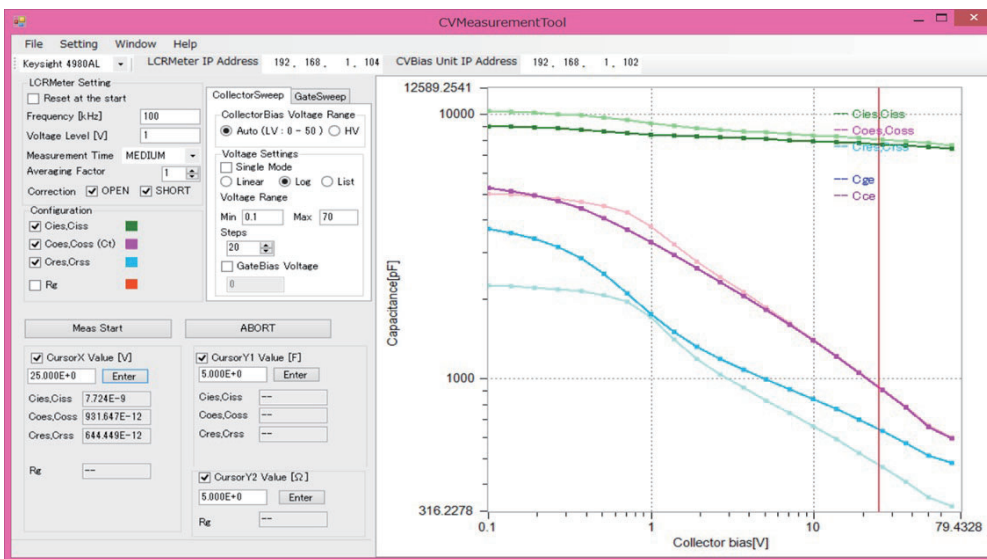
	CS-605A	CS-603A
DC biasing range	0-5kV / 0-50V	0-3kV / 0-50V
Setting Resolution	100mV / 1mV	
Measurement range	$\leq 3.6\text{nF}$ (2%) / $\leq 1\mu\text{F}$ (2%)	$\leq 4\text{nF}$ (2%) / $\leq 1\mu\text{F}$ (2%)
Frequency range	1kHz-1MHz	
DC blocking C AC Shorted C	$\geq 180\text{nF}$ / $\geq 50\mu\text{F}$	$\geq 200\text{nF}$ / $\geq 50\mu\text{F}$
Measurement parameters	Cies, Ciss (Input capacitance) , Coes, Coss (Output capacitance) , Cres , Crss (Reverse transfer capacitance) , CT (Capacitance between terminals) , Cgs,Cge/Cgd,Ccg/Cds,Cce (Calculated) , Rg (Gate resistance)	
Measurement Mode	C-V: Capacitance vs Bias voltage, C-G: Capacitance vs Gate voltage C-Time: Capacitance vs time	
Gate bias	+/-25V at 1mV/step (Sweep function available)	
Type of sweeps	Linear / Log / List / Single	
Sweep direction	UP Sweep	
Measurement points	5000 points / 5000 points	5000 points / 5000 points
Others	Correction (Open/Short) , Auto ranging, Real-time measurement , Waveform comparison , REF display, Interlock function (Standard) , External Interlock function	
Dimensions	Approx. 330W×370D×230H (mm)	

CV Measurement Tool (Flee software)



Example of test result up to 2.5kV

- - Cies, Ciss
- - Coes, Coss
- - Cres, Crss



Example of detailed test up to 70V

- - Cies, Ciss (with comparison)
- - Coes, Coss (with comparison)
- - Cres, Crss (with comparison)

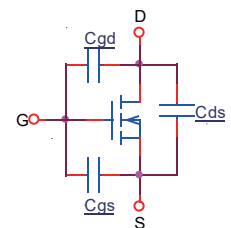
Definitions

Input capacitance : $C_{iss} = C_{gs} + C_{gd}$
 Output capacitance : $C_{oss} = C_{ds} + C_{gd}$
 Reverse transfer capacitance : $C_{rss} = C_{gd}$

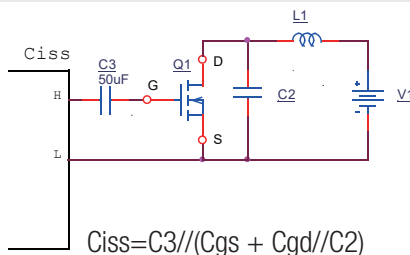
Measurement block diagrams

Q1 : DUT

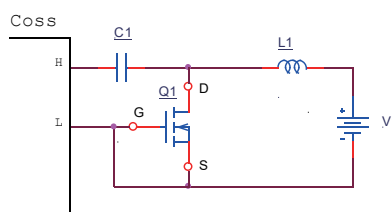
$V_1 = 50V$ $C_1, C_2, C_3 \geq 50 \mu F$
 $V_1 = 3kV$ $C_1, C_2 \geq 200nF, C_3 \geq 50 \mu F$
 $V_1 = 5kV$ $C_1, C_2 \geq 180nF, C_3 \geq 50 \mu F$



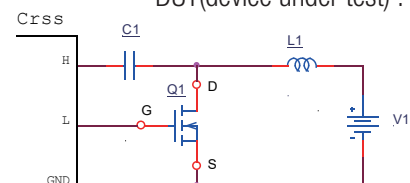
DUT(device under test) : Q1



$$C_{iss} = C_3 // (C_{gs} + C_{gd} // C_2)$$



$$C_{oss} = C_1 // (C_{ds} + C_{gd})$$



$$C_{rss} = C_1 // C_{gd}$$

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